

**What Is Claimed Is:**

1 1. An electrostatic discharge (ESD) protection circuit with low  
2 input capacitance, suitable for an I/O pad, comprising a  
3 plurality of diodes, stacked and coupled between a first  
4 power line and the I/O pad, wherein during normal operation,  
5 the diodes are reverse-biased, and, when an ESD event occurs  
6 between a second power line and the I/O pad, the diodes are  
7 forward-biased to conduct ESD current.

1 2. The ESD protection circuit as claimed in claim 1, wherein each  
2 diode is a PN junction diode formed by placing a doped area  
3 of a first conductivity type in a first well of a second  
4 conductivity type, a deep well of the first conductivity type  
5 formed under the first well to isolate the first well from  
6 a substrate of the second conductivity type.

1 3. The ESD protection circuit as claimed in claim 2, wherein the  
2 first well is surrounded by a second well of the first  
3 conductivity type.

1 4. The ESD protection circuit as claimed in claim 2, wherein the  
2 first conductivity type is N type, and the second  
3 conductivity type is P type.

1 5. The ESD protection circuit as claimed in claim 1, wherein the  
2 ESD protection circuit further includes a power-rail ESD  
3 clamp circuit, set between a first power line and a second  
4 power line, the power-rail ESD clamp circuit being turned on  
5 to conduct ESD current when an ESD event occurs.

1 6. The ESD protection circuit as claimed in claim 5, wherein the  
2 power-rail ESD clamp circuit includes a substrate-triggered  
3 MOS of the first conductivity type, the substrate-triggered  
4 MOS including two source/drains and a substrate, the two  
5 source/drains coupled to the first power line and the second  
6 power line respectively, the substrate node biased with  
7 suitable current to trigger a bipolar junction transistor  
8 parasitizing in the substrate-triggered MOS, and conducting  
9 ESD current when an ESD event occurs.

1 7. The ESD protection circuit as claimed in claim 6, wherein the  
2 substrate-triggered MOS includes a gate applied with a first  
3 bias voltage to keep the substrate-triggered MOS off during  
4 normal operations.

1 8. The ESD protection circuit as claimed in claim 6, wherein the  
2 gate is applied with a second bias voltage to speed up the  
3 turn-on rate of the substrate-triggered MOS when an ESD event  
4 occurs.

1 9. The ESD protection circuit as claimed in claim 6, wherein the  
2 substrate-triggered MOS is formed in a first well of a second  
3 conductivity type, a deep well of a first conductivity type  
4 being formed under the first well to isolate the first well  
5 from a substrate of the second conductivity type.

1 10. The ESD protection circuit as claimed in claim 9, wherein the  
2 first well is surrounded by a second well of the first  
3 conductivity type.

1 11. The ESD protection circuit as claimed in claim 5, wherein the  
2 power-rail ESD clamp circuit includes an ESD detection  
3 circuit to detect the occurrence of the ESD event.

1 12. The ESD protection circuit as claimed in claim 1, wherein one  
2 of the diodes is a MOS diode with a gate coupled to a  
3 source/drain of the MOS diode.

*Sub 12*  
1 ~~13. The ESD protection circuit as claimed in claim 1, wherein the~~  
2 ~~diode includes a PN junction diode formed by a PN junction~~  
3 ~~between a source/drain and a substrate of a MOS.~~

1 14. The ESD protection circuit as claimed in claim 13, wherein  
2 the gate of said MOS is coupled to the first power line.

*Sub 13*  
1 ~~15. The ESD protection circuit as claimed in claim 13, wherein~~  
2 ~~the gate of said MOS is coupled to another source/drain of~~  
3 ~~the MOS.~~

1 16. The ESD protection circuit as claimed in claim 13, wherein  
2 the MOS is PMOS.

1 17. The ESD protection circuit as claimed in claim 13, wherein  
2 the MOS is NMOS.

1 18. A power-rail ESD clamp circuit, suitable for an integrated  
2 circuit, coupled between two power lines, comprising:  
3 a substrate-triggered MOS, including:  
4 a gate;

two source/drains, respectively coupled to two power lines; and  
a substrate; and  
an ESD detection circuit, providing a bias current to the substrate of the MOS, and a bias voltage to the gate of the MOS element to trigger the MOS and conduct ESD current when an ESD event occurs.

19. The power-rail ESD clamp circuit as claimed in claim 18, wherein the power-rail ESD clamp circuit further comprises a voltage clamp circuit coupled between the gate and one of the two power lines to limit the bias voltage.

20. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by one diode forward-biased when the ESD event occurs.

21. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by a plurality of stacked diodes forward-biased when the ESD event occurs.

22. The power-rail ESD clamp circuit as claimed in claim 19, wherein the voltage clamp circuit is formed by a Zener diode reverse-biased to clamp the bias voltage at a breakdown voltage when ESD event occurs.

23. The power-rail ESD clamp circuit as claimed in claim 18, wherein one of the two power lines is a high voltage power line, the other is a low voltage power line, and the substrate-triggered MOS is an NMOS.

1 24.The power-rail ESD clamp circuit as claimed in claim 18,  
2 wherein said ESD detection circuit comprising:  
3 an RC-based circuit for detecting the ESD event; and  
4 a driver controlled by the RC-based circuit, for driving the  
5 gate and the substrate of the substrate-triggered MOS.

1 25.The power-rail ESD clamp circuit as claimed in claim 24,  
2 wherein the RC-based circuit includes a resistor and a  
3 capacitor, connected in series between the two power lines.

1 26.The ESD clamp circuit between power lines as claimed in claim  
2 24, wherein the driver includes an inverter, having an output  
3 node coupled to the gate and the substrate of the  
4 substrate-triggered MOS.